AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph at page 4, line 15, with the following rewritten paragraph:

When the main power source 2 is turned on, the power supply circuits 3 to 7 transform a power supply voltage which is supplied from the main power source 2 into arbitrary power supply voltages VDD1 to VDD5, and supply these voltages to the multiple power source semiconductor integrated circuit 1g. The multiple power source semiconductor integrated circuit 1g receives the power supply voltages VDD1 to VDD5 which are supplied from the power supply circuits 3 to 7 through the corresponding external power supply terminals 21 to 25. The power which is received through the external power supply terminals 21 to 25 is supplied to the function blocks 11 to 14 and the [input] input/output terminal circuit 15 via the internal power supply lines 31 to 35. The respective function blocks 11 to 14 and the input/output terminal circuit 15 execute respective processing for implementing prescribed functions.

Please replace the paragraph at page 19, line 18, with the following rewritten paragraph:

The power supply that is received through the fifth external power supply terminal 25 is supplied to the ~~input~~ input/output terminal circuit 15 and the power supply control circuit 40 via the fifth internal power supply line 35, and the power supply that is received through the first external power supply terminal 21 is supplied to the first function block 11 via the first internal power supply line 31. Similarly, the power supply that is received through the second external power supply terminal 22 is supplied to the second function block 12 via the second internal power supply line 32, the power supply that is received through the third external power supply terminal 23 is supplied to the third function block 13 via the third internal power supply line 33, and the power supply that is received through the fourth external power supply terminal 24 is supplied to the fourth function block 14 via the fourth internal power supply line 34, respectively.

Please replace the paragraph at page 23, line 12, with the following rewritten paragraph:

The multiple power source semiconductor ~~device~~ integrated circuit 1a according to the second embodiment includes a power supply control circuit 40a that is provided with a register ~~61~~ 62 for holding data of the first interrupt signal (which is shown as a first power recover signal in figure 3) 55, and a register ~~62~~ 61 for holding data of the second interrupt signal (which is shown as a second power recover signal in figure 3) 56, and the register 61 and the first function block 11 are connected by an internal signal 63, and the register 62 and the first function block 11 are connected by an internal signal 64, respectively.

Please replace the paragraph at page 23, line 25, with the following rewritten paragraph:

When supply of power is restarted by the first interrupt signal 55 or the second interrupt signal 56 while the supply of power to the first to fourth function blocks 11 to 14 is halted (when the respective function blocks are on standby), the registers ~~61~~ 62 and ~~62~~ 61 hold data of the first and second interrupt signals 55 and 56, respectively. When the supply of power is restarted, the first function block 11 obtains the data that are held in the internal registers 61 and 62 via the internal signal 63 and 64, to check contents of the interrupt control.

Please replace the paragraph at page 24, line 9, with the following rewritten paragraph:

As described above, according to the multiple power source semiconductor integrated circuit 1a of the second embodiment, the register ~~61~~ 62 for holding data of the interrupt signal 55 and the register ~~62~~ 61 for holding data of the interrupt signal 56 are provided in the power supply control circuit 40a, and the register 61 and the first function block 11 are connected by the internal signal 63, and the register 62 and the first function block 11 are connected by the internal signal 64, respectively. Therefore, when a standby state in which the supply of power is halted is released by some key operation (interrupt control) to restart the supply of power to the first to fourth function blocks 11 to 14, the first function block 11 checks contents of the key operation by checking the data

that are held in the register 61 or 62, thereby executing a predetermined operation in accordance with the key operation.

Please replace the paragraph at page 25, line 12, with the following rewritten paragraph:

In a multiple power source semiconductor ~~device~~ integrated circuit 1b according to the third embodiment, the second function block 12 includes a CMOS inverter circuit 74 for generating a inter-block signal 72, and the first function block 11 includes a two-input OR circuit 71 that outputs an OR between the power cutoff signal 42 and the inter-block signal 72 that is outputted from the second function block 12 as the internal signal 73, to fix the inter-block signal 72 from the second function block 12 when supply of power to the second function block 12 is stopped.

Please replace the paragraph at page 30, line 7, with the following rewritten paragraph:

In the multiple power source semiconductor ~~device~~ integrated circuit 1c according to the fourth embodiment, the first function block 11 includes a first inverter circuit 81, and a two-input NOR circuit 82 that outputs a NOR between an output from the first inverter circuit 81 and a power cutoff signal 42 as an inter-block signal 84, to fix the inter-block signal 84 to the second function block 12 at "L" level when power supply to the second function block 12 is halted, and the second function block 12 includes a second inverter circuit 86 to which the inter-block signal 84 from the first function block 11 is inputted.

Please replace the paragraph at page 38, line 19, with the following rewritten paragraph:

An output 103 of the input terminal 100, an input 104 of the first output terminal 101, and an input 105 of the second output terminal 102 are respectively connected to the first function block 11 which is a microcomputer for controlling the system. Further, switching circuits 107 to 109 to which a terminal hold signal 106 that is outputted from the power supply control circuit ~~40~~ 40e is

inputted, to switch signal levels in accordance with the inputted terminal hold signal 106 are provided in the terminals, respectively.

Please replace the paragraph at page 43, line 23, with the following rewritten paragraph:

The main power cutoff circuit 131 is constituted, for example, by an FET (Field Effect Transistor), and has a structure of stopping respective supply of power to the power supply circuits 3 to 7 in accordance with a "H" level output of the power cutoff signal ~~4f~~ 410.